Improving Through-Silicon Via Reliability in 3-D Integrated Circuits Using EBSD

Materials Challenge

Three-dimensional integrated circuits (3-D IC) have emerged as a promising route for high performance systems to meet the growing demands of mobile computing. Through-silicon vias (TSV) connect multiple device levels into a single integrated circuit. This approach eliminates edge wiring requirements, reduces the electrical path-length, provides faster device operation, and reduces power consumption. The reliability of copper TSVs depends on both deposition conditions and the thermal loading used during the 3-D IC manufacturing process. Optimization of both the deposition and thermal annealing conditions is important for maximizing device lifetime.

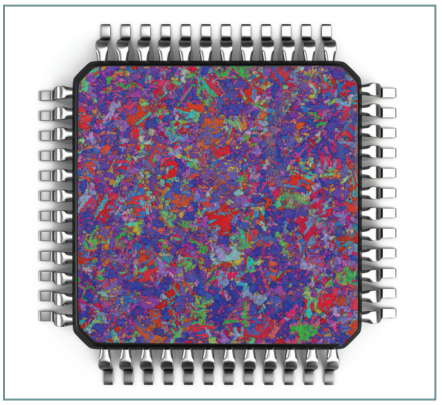
Comparison with Existing Solutions

Analyzing microstructural changes that occur due to processing conditions during device fabrication can be a predictor of the reliability of TSVs in 3-D ICs. The microstructural features of interest can be observed using a combination of characterization techniques:

- **Focused Ion Beam (FIB).** FIB images provide qualitative information on grain size and TSV deposition and filling quality through crystallographic channeling imaging. FIB imaging does not provide direct crystallographic orientation information or quantitative grain size determination. Crystal orientation provides feedback on the deposition process while grain size provides information on the annealing process.

- **Transmission Electron Microscopy (TEM).** TEM provides crystallographic-based imaging of grains and defects within a TSV. These images provide qualitative microstructural details; however, the determination of the crystallographic orientation in the TEM is generally done manually. This limits the number of quantitative measurements thereby making statistically reliable sampling difficult for grain size and preferred orientation determination.

- **Nanoindentation.** Nanoindentation characterizes material response on a sub-micrometer scale to provide information on yield strength and elastic moduli giving insight into the grain size and plastic strain present within the TSVs. Microstructural features such as crystal orientation and composition can change the local strength and strain values measured; however, without direct knowledge of this local microstructure the variance in measured values cannot be accurately explained.



In contrast, Electron Backscattered Diffraction (EBSD) provides a fast and automated solution to characterize the microstructure of copper TSVs. The advantages of EBSD are:

- Direct measurement of grain size through discrete crystallographic orientation measurements removes ambiguity in grain determination. Copper grain size can be measured after deposition and after thermal cycling to adjust the manufacturing parameters to control grain size distribution and obtain complete TSV fill.

- Direct measurement of crystallographic orientation and texture provides an understanding of the copper film deposition process. Variables such as bath additives, voltage, and deposition rate determine the preferred orientation that develops and influences the fill rate and probability of void formation.

- Direct measurement of intergranular misorientations that form within the TSV copper. These misorientations indicate plastic deformation has occurred during thermal cycling. The presence of plastic deformation indicates that copper protrusions may form which cause reliability concerns with cracking and delamination.

Microanalysis Results

EBSD data was collected from a 6μm x 40μm copper TSV after deposition and thermal cycling simulating back-end-of-line (BEOL) processing. Figure 1 shows an orientation map with orientations colored relative to the sidewall growth direction. The EBSD data reveals a recrystallized structure with a large number of twin boundaries with no significant preferred orientation development. Good TSV fill is also observed. The average grain size is 978 nm. Twin boundaries provide significantly slower diffusion pathways through the TSV relative to random high-angle grain boundaries. A twin-adjusted grain size of 2.72μm is measured if twin boundaries are excluded from the grain determination algorithm. This adjusted grain size will better predict the reliability.

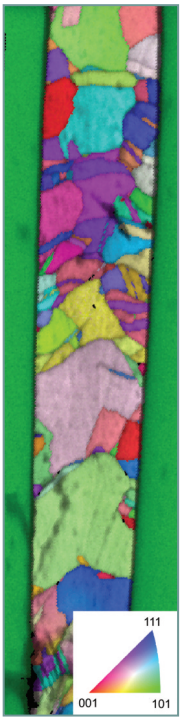


Figure 1 - Orientation map of copper through-silicon via showing no preferred orientation.

Figure 2 shows the grain structure, including and excluding twins, where the grains are randomly colored to show size and morphology. The grain structure excluding twins is closer to the desired "bamboo" structure, where the high-angle boundaries are generally close to perpendicular to the length of the TSV. This grain structure limits the possible grain boundary diffusion paths through the TSV and will provide greater electromigration failure resistance.

Figure 3 shows a Kernel Average Misorientation (KAM) map with coloring corresponding to the level of plastic deformation present in the copper TSV. During thermal cycling, the coefficient of thermal expansion differences between the copper and surrounding silicon wafer cause stresses to occur. When these stresses exceed the elastic limit of the copper, permanent plastic deformation will occur. This deformation may lead to copper protrusions from within the TSV that can manifest as reliability issues within the device.

Figure 2 - Grain maps of copper TSV with twin boundaries included and excluded from grain.

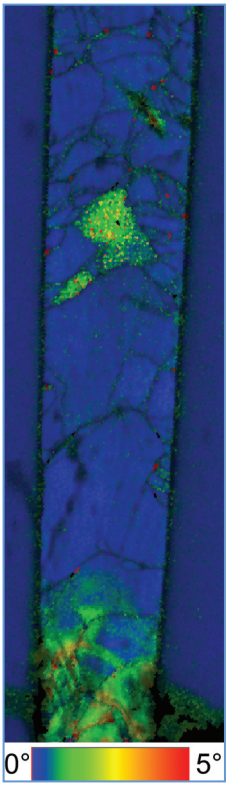


Figure 3 - Kernel average misorientation map showing the plastic strain developing after thermal cycling, which can reduce reliability.

The KAM map shows that a region of plastic deformation has developed at the bottom of this TSV. In this case, thermal cycling variables should be adjusted to reduce the applied stress in order to improve reliability.

Recommended EDAX Solution

TEAM™ Pegasus Analysis Systems are recommended to help engineers develop deposition and thermal cycling manufacturing procedures for reliable copper TSVs in 3-D IC applications. TEAM™ Pegasus Analysis Systems offer integrated EDS and EBSD characterization with an easy to use interface for fast analysis of grain size, grain orientation, phase distribution, and texture. Hikari XP EBSD cameras provide fast, sensitive, and smart EBSD pattern collection with superior orientation precision for measuring plastic deformation within stressed TSVs.